

CISC 6200 Computer Organization

Assignment 4

Out 11/3; Due 11/17

- Q1. (a) What programming conventions relate to the use of the s, a, and v registers in MIPS?
(b) What special function do the ra and sp registers perform in MIPS?
- Q2. (a) You need to save the values in the a0, a1, and s0 registers on the stack, write MIPS assembler to do this
(b) You need to restore the values you saved above from the stack back into the registers, write MIPS assembler to do this
- Q3. (i) Calculate the time necessary to perform a multiply using the algorithm in section 3.3 of the text (the shift and add algorithm covered in class) if an integer is A bits wide and each step of the operation takes B time units. You can assume that an addition step is always done (either a 0 or a copy of the multiplicand). You can also assume that all the registers have been loaded and are ready to go and that the algorithm is being performed in software.
(ii) If this is being done in hardware then the shifts of multiplier and multiplicand can be done in parallel. How would this affect the time?

(iii) Consider the parallel implementation of multiplication covered in class and at the end of section 3.3 in the text. Calculate the time necessary with that method to perform a multiply if an integer is A bits wide and each adder takes B time units.
- Q4. Consider the following two bit patterns:
- a. 0x24A60004
 - b. 0xAFBF0000
- (i) What decimal number does each of (a) and (b) represent if it is a two's complement integer?
 - (ii) What decimal number does each of (a) and (b) represent if it is an unsigned integer?
 - (iii) If each of (a) and (b) is placed into the Instruction Register, what MIPS instruction will execute?
 - (iv) What decimal number does each of (a) and (b) represent if it is a floating point number (IEEE 754 standard)?
- Q5. Consider the following two numbers:
- a. -1609.5
 - b. -938.8125
- (i) Write down the binary representation of each of (a) and (b) in IEEE 754 single precision format.
 - (ii) Write down the binary representation of each of (a) and (b) in IEEE 754 double precision format.